AMENDMENTS TO THE SPECIFICATION

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph beginning at page 11, line 14 with the following paragraph:

A local oscillator clock (e.g., OSC2_IW_PH) to the mixers 170 and 178 may be at 1024MHz, which implies that the image channel for the mixers 170 and 178 may be located at 724MHz. The filter ~~176~~ 164 may eliminate or substantially attenuate signal content at 724MHz, which is possible to achieve with a filter Q of about 20. Such a filter considerably reduces the performance needed for implementing the filter ~~176~~ 164 when compared to the filter in the dual conversion tuner architecture 20 of the background section. In addition, a filter with Q of around 20 could be achieved by low cost passive components and also lends to being integrated onto the same integrated circuit as the mixer 162.

Please replace the paragraph beginning at page 12, line 1 with the following paragraph:

To further improve the image rejection capability, the mixers 170 and 178 may be implemented as an image reject type filter. The input signal may be mixed in two separate signal

paths, with the local oscillator clocks OSC2_IW_PH and OSC2_QUAD phased in quadrature relationship in the two paths. A quadrature relationship may allow the signals OSC2_IW_PH and OSC2_QUAD to be phased 90 degree apart in the two signal paths. After the quadrature mixing process (e.g., the mixers 170 and 178), each of the two signal paths may be combined at the summation circuit 174 and filtered at the filter 176 to form the signal IF2'. A more detailed explanation can be found in ~~co-pending~~ application Serial No. ~~_____ (Attorney Docket No. 1496.00114)~~ 09/880,290, filed 6/13/2001, now abandoned. The mixers 190 and 192 may then downcovert the IF2' signal to 44MHz, by mixing with the third local oscillator signals OSC3_IW_PH and OSC3_QUAD located at a frequency of 256MHz.